REMARKS

In the Official Action mailed 11 January 2007, the Examiner rejected claims 1-2, 4-6, 11-15, 17, 20-21, 23-25 and 28-30 under 35 U.S.C. §102(e); rejected claims 3 and 22 under 35 U.S.C. §103(a); rejected claims 7-8, 18-19 and 31-32 under 35 U.S.C. §103(a); rejected claims 9 and 26 under 35 U.S.C. §103(a); rejected claims 10 and 27 under 35 U.S.C. §103(a); and rejected claim 16 under 35 U.S.C. §103(a).

Claims 1-32 remain pending.

Rejection of Claims 1-2, 4-6, 11-15, 17, 20-21, 23-25 and 28-30 under 35 U.S.C. §102(e)

The Examiner has rejected claims 1-2, 4-6, 11-15, 17, 20-21, 23-25 and 28-30 under 35 U.S.C. §102(e) as being anticipated by Ikeda et al. (US 2003/0184339) (hereinafter referred to as "Ikeda"). Applicant respectfully requests reconsideration.

For at least the reasons stated below, Applicant asserts that Ikeda fails to expressly or inherently describe each and every element of the invention claimed by Applicant.

Independent Claim 1: Independent claim 1 of the present invention –

> An integrated circuit, comprising:
>
> an input port by which data is received from a source external to the integrated circuit;
>
> a configurable logic array having a programmable configuration defined by configuration data stored in electrically programmable configuration points within the configurable logic array;
>
> memory storing instructions for a mission function for the integrated circuit, storing instructions for a configuration load function used to receive configuration data via said input port, and storing instructions for a configuration function used to transfer the configuration data to the programmable configuration points within the configurable logic array; and
>
> a processor coupled to the memory which fetches and executes said instructions from the memory.

In the rejection of claim 1, the Examiner states that Ikeda teaches "a configurable logic array (i.e. the Offchip FPGA in Fig. 1) having a programmable configuration defined by configuration data stored in electrically programmable configuration points within the configurable logic array" and "memory (i.e. the RAM or ROM for storing the execution program 3 shown in Figure 1)... storing instructions for a configuration load function..., and storing instructions for a configuration function..." (Office Action, page 3).

Applicant respectfully submits that it is incorrect to read the configurable logic array of claim 1 on the "Offchip FPGA" of Ikeda. Further, the Examiner has not associated an element of Ikeda with the "configuration load function" or the "configuration function" of claim 1. As explained below, Applicant submits that Ikeda does not disclose storing instructions for a "configuration load function".

Ikeda does not disclose the manner in which the Offchip FPGA is programmed. Thus, Ikeda does not disclose a configuration function or configuration load function associated with the FPGA. Ikeda only discloses that the FPGA supports a programmable matrix (Ikeda, Figure 1, ref. no. 20) in the processing of data. See, Ikeda, Figures 1 and 11(a), and paragraphs [0052] and [0077]. Additionally, Ikeda discloses that an advantage of his invention of programming a matrix instead of programming the FPGA is "[w]ith this integrated circuit device, there is no need to change all the connections at the transistor level as is the case with an FPGA, so that the hardware can be reconfigured in a short time." (Ikeda, paragraph [0005]).

One could take the position that the programmable logic array of claim 1 of the present invention reads on the matrix disclosed by Ikeda. Ikeda does describe configuring the matrix. However, even if one takes the position that the programmable logic array of claim 1 reads on the matrix disclosed by Ikeda, Applicant submits that claim 1 of the present invention is patentably distinct from Ikeda because Ikeda does not describe a "configuration load function".

Ikeda discloses two ways in which the matrix is configured. As is described below, neither way includes memory storing instructions for a configuration load function to receive configuration data via an input port.

The first way disclosed by Ikeda is found in paragraph [0088]. The operation units and switching units of the matrix each include "a configuration memory by which these units are separately controlled by setting data from the processor 11. Accordingly, the configuration of the operation units 30 can be freely changed by the processor...". Ikeda in paragraph [0111]

describes in more detail how the configuration is controlled by the processor when Ikeda discloses that instructions are incorporated directly into the execution program stored in memory and that the processor controls the configuration of the matrix according to the instructions in the execution program. Ikeda does not disclose storing and executing any instructions related to "a configuration load function used to receive configuration data via said input port", as required by claim 1.

The second way of configuring the matrix in Ikeda is found in paragraphs [0100]-[0107] and in Figure 14. This second way is a multi-step process of configuring the operation units which, as described in more detail below, is based on external manual input or software used during the design and manufacture of the circuit. The process begins by providing a specification 71 containing the processing to be executed by the LSI 10 and that a conversion process 72 for converting the specification is "performed manually, or may be executed using software such as a compiler" (Ikeda paragraph [0100] lines 13-15). A next step in this process involves a place-and-route process, in which Ikeda discloses "in the place-and-route process 75, it is necessary to generate an execution configuration that includes the configurations of the internal data paths 32 of the operation units that are combined. The settings of the operation units 30 are supplied to the matrix 20..." (Ikeda paragraph [0107] lines 6-13). Thus, Ikeda discloses that resources external to the integrated circuit initiate the process for transferring configuration data from outside the integrated circuit to the matrix based on external manual input or software such as a compiler, and not based on instructions for a configuration load function stored in memory on the integrated circuit that are executed by the processor.

Therefore, claim 1 is patentably distinct from Ikeda for at least the reasons that no configuration function or configuration load function is associated with the Offchip FPGA and no configuration load function is associated with the matrix.

Claims 2, 4-6, 11-15, and 17 depend from claim 1, and are patentable for at least the same reasons as claim 1.

In the rejection of independent claim 20, the Examiner states "As per claims 20-21, 23-25, and 28-30, see arguments with respect to the rejection of claims 1-2, 4-6 and 11-13, respectively. Claims 20-21, 23-25, and 28-30 are also rejected based on the same rationale as the rejection of claims 1-2, 4-6 and 11-13, respectively." (Office Action, pages 4-5).

Claim 20, in part, states "storing instructions in a second memory array of said memory for configuration load function used to receive configuration data from a source external to the integrated circuit". As is stated above with respect to claim 1, Ikeda does not disclose storing instructions for a configuration load function.

Therefore, for at least the reasons stated above, claim 20 is patentably distinct from Ikeda. Claims 21, 23-25, and 28 depend from claim 20, and are patentable for at least the same reasons.

Accordingly, reconsideration of the rejection of claims 1-2, 4-6, 11-15, 17, 20-21, 23-25 and 28-30 is respectfully requested.

Rejection of Claims 3 and 22 under 35 U.S.C. §103(a)

The Examiner has rejected claims 3 and 22 under 35 U.S.C. §103(a) as being unpatentable over Ikeda in view of Hsu et al. (US 5359570).

Claim 3 depends from claim 1, and claim 22 depends from claim 20, and therefore such claims are patentable for at least the reasons discussed above and because of the unique combinations recited.

Accordingly, reconsideration of the rejection of claims 3 and 22 is respectfully requested.

Rejection of Claims 7-8, 18-19 and 31-32 under 35 U.S.C. §103(a)

The Examiner has rejected claims 7-8, 18-19 and 31-32 under 35 U.S.C. §103(a) as being unpatentable over Ikeda in view of Sun et al. (US 6401221).

Claims 7 and 8 depend from claim 1, and claims 31 and 32 depend from claim 20, and therefore such claims are patentable for at least the reasons discussed above and because of the unique combinations recited.

The Examiner states that independent claim 18 is "rejected based on the same rationale as the rejection of claim 8." (Office Action, page 6). Claim 8 depends from claim 1 and both claim 1 and claim 18 include a "configuration load function".

In rejecting claim 8 the Examiner relies on the combination of Ikeda and Sun and states that "Ikeda teaches that the claim invention as described above, but failed to teach the watchdog time as claimed." Thus, the Examiner is taking the position that Ikeda teaches the "configuration load function" of claim 18.

As is stated above with respect to claim 1, Ikeda does not disclose storing instructions for a configuration load function. Therefore, claim 18 is patentable for at least the same reasons as claim 1.

Claim 19 depends from claim 18 and is patentable for at least the same reasons.

Accordingly, reconsideration of the rejection of claims 7-8, 18-19 and 31-32 is respectfully requested.

Rejection of Claims 9 and 26 under 35 U.S.C. §103(a)

The Examiner has rejected claims 9 and 26 under 35 U.S.C. §103(a) as being unpatentable over Ikeda in view of Sun et al. (US 5901330).

Claim 9 depends from claim 1, and claim 26 depends from claim 20, and therefore claims 9 and 26 are patentable for at least the reasons discussed above and because of the unique combinations recited.

Accordingly, reconsideration of the rejection of claims 9 and 26 as is respectfully requested.

Rejection of Claims 10 and 27 under 35 U.S.C. §103(a)

The Examiner has rejected claims 10 and 27 under 35 U.S.C. §103(a) as being unpatentable over Ikeda in view of Lawman (US 6028445).

Claim 10 depends from claim 1, and claim 27 depends from claim 20, and therefore such claims are patentable for at least the reasons discussed above and because of the unique combinations recited.

Accordingly, reconsideration of the rejection of claims 10 and 27 is respectfully requested.

Rejection of Claim 16 under 35 U.S.C. §103(a)

The Examiner has rejected claim 16 under 35 U.S.C. §103(a) as being unpatentable over Ikeda in view of Akao et al. (US 5900008).

Claim 16 depends from claim 1, and therefore is patentable for at least the reasons discussed above and because of the unique combination recited.

Accordingly, reconsideration of the rejection of claim 16 is respectfully requested.

CONCLUSION

It is respectfully submitted that this application is now in condition for allowance, and such action is requested.

The Commissioner is hereby authorized to charge any fee determined to be due in connection with this communication, or credit any overpayment, to our Deposit Account No. 50-0869 (MXIC 1520-1).

Respectfully submitted,

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